

MODELS 108/116 DISPLAY CONTROL ACCESSORIES

PRELIMINARY

This preliminary manual is intended to be delivered with the instrument. Detailed information will be provided in a final operating manual.

Under normal circumstances, all owners of Biomation Display Control Accessories who receive this preliminary manual should return it to Biomation for a final version.

OPERATING AND SERVICE MANUAL

IF FOR SOME REASON A FINAL EDITION IS NOT RECEIVED PLEASE CONTACT THE BIOMATION FACTORY, GIVE THE SERIAL NUMBER OF THE UNIT AND COMPLETE RETURN ADDRESS INFORMATION.

biomation

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INTRODUCTION

To avoid confusion, the 108/116 manual was written using only the 116 accessory to the 1650-D Logic Analyzer. Keep in mind, however, that the operation and features of the 116 Display Control unit are identical to the 108 unit (for the Model 851-D), except for the width of the data field.

IMPORTANT NOTE

This preliminary manual is supplied to permit earliest possible delivery of instruments. Additional and more complete information will be included in a subsequent final edition of this manual.

Under normal circumstances, all owners of Model 108/116 Display Control Accessories who receive this preliminary manual with their unit will automatically receive a copy of the final edition.

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OPERATING AND SERVICE MANUAL
MODEL 108/116

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SECTION I
OPERATING AND SERVICE MANUAL
MODEL 108/116

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1.1 Description

The Model 116 Display Control Accessory extends the Model 1650-D Logic Analyzer as an analytical tool, formatting the 320 bit memory for time or data analysis. This combined unit becomes a single powerful tool for analysis of today's complex digital circuits and detailed firmware.

The Display Control provides three output modes for the data recorded in the analyzer's solid state memory. These are: Timing Diagram (useful for hardware troubleshooting); Data Dump with address location, truth table, etc.; plus hexadecimal or octal translation (for program analysis). There is also a Dump Mode, which translates each digital word into its equivalent dot position on the CRT (for both Firmware and hardware analysis).

SECTION I

GENERAL INFORMATION

1.1 Certification

Biomation Corporation certifies that this instrument accessory was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory.

1.2 Warranty

All Biomation products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products that prove to be defective during the warranty period. If a unit fails within thirty days of delivery, Biomation will pay all shipping charges relating to the repair of the unit. Units under warranty, but beyond the thirty day period, should be sent to Biomation prepaid and Biomation will return the unit prepaid. Units out of the one year warranty period, the customer will pay all freight charges. IN THE EVENT OF A BREACH OF BIOMATION'S WARRANTY, BIOMATION SHALL HAVE THE RIGHT IN ITS DISCRETION EITHER TO REPLACE OR REPAIR THE DEFECTIVE GOODS OR TO REFUND THE PORTION OF THE PURCHASE PRICE APPLICABLE THERETO. THERE SHALL BE NO OTHER REMEDY FOR BREACH OF THE WARRANTY. IN NO EVENT SHALL BIOMATION BE LIABLE FOR THE COST OF PROCESSING, LOST PROFITS, INJURY TO GOODWILL, OR ANY SPECIAL OR CONSEQUENTIAL DAMAGES. THE FOREGOING WARRANTY IS EXCLUSIVE OF ALL OTHER WARRANTIES, WHETHER EXPRESSED OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

1.3 Description

The Model 116 Display Control Accessory extends the Model 1650-D Logic Analyzer as an analytical tool, formatting the 500 bit memory for time or data analysis. This combined unit becomes a single powerful tool for analysis of today's complex digital circuits and detailed firmware.

The Display Control provides three output modes for the data recorded in the analyzer's solid state memory. These are: Timing Diagram (useful for hardware troubleshooting); Data Domain with address location, truth table format, plus hexadecimal or octal translation (for program analysis); and Map Mode, which translates each digital word into a unique dot on the CRT (for both firmware and hardware analysis).

The accessory is composed of a replacement cover for the Model 1650-D which contains switch selectable formatting for the 1650-D memory, and a separate hold memory with related comparison logic. The Model 116 conveniently interconnects to the 1650-D via three supplied BNC cable connections and a supplied digital interface cable and connector.

1.4 Specifications

DISPLAY MODES

Timing Diagram. Gates 1650-D timing diagram output format to the display. Expansion, cursor, and channel output selection controllable from 1650-D front panel.

Data Domain. Presents 16 sample words of the recorded data starting from the cursor location when the 500 sample "A" memory is selected or the entire contents of the hold "B" memory. The data memory location, binary data bits, and selectable hexadecimal or octal translation appear on this display format.

Map Mode. Switch selectable map of entire 500 word 1650-D memory "A" or 16 word hold memory "B".

Compare. Allows comparison of 16 words starting from the cursor address location with the 16 words stored in the "B" hold memory. Function in Data Domain and Map formats. Differences blink.

Stop A ≠ B. Operates in conjunction with the Delayed Auto Record Mode of the 1650-D continuously comparing the newest record update (16 words from the constant cursor position) with that data stored in the "B" memory. When "A" no longer coincides with "B," the auto update process halts and the differences blink on the display.

X Output: +1 V F.S., 200 ohms output impedance.

Y Output: +1 V F.S., 200 ohms output impedance.

Z Output: +22 V F.S., 1K ohms output impedance.

\bar{Z} Output: +4 V F.S., 270 ohms output impedance.

Interconnection to Model 1650-D. Simple connection of the three supplied BNC connections to the X, Y, and Z outputs of the Logic Analyzer and connection of a digital interface cable and connector are required for installation of the Model 116.

Model 108

Height: 2.0"
Length: 18.0"
Width: 12.75"
Weight: Approx. 8 lbs.

Model 116

2.0"
18.0"
17.0"
Approx. 8.5 lbs.

Display Control Assembly

2.2 Unpacking and Inspection

Inspect accessory for shipping damage as soon as it is unpacked. Check for broken connectors; inspect cabinet and panel surfaces for dents and scratches. If the accessory is damaged in any way or fails to operate properly, notify the carrier immediately. For assistance of any kind, including help with instruments under warranty, contact your local Biomation representative or Biomation in Cupertino, California, U.S.A.

2.3 Storage and Shipment

To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Contract packaging companies in many cities can provide dependable custom packaging on short notice.

2.4 Connections

For 1650-D and 116 units that are shipped together, six connections were made at the factory. Compare the unit with Figure 2.1 to ensure that shipment has not disturbed the connections.

Installation of the 116 Display Control on existing Model 1650-D Logic Analyzers requires a Phillips screwdriver to remove the existing top cover and to replace it with the accessory cover.

CAUTION: UNPLUG THE 1650-D BEFORE REMOVING THE TOP COVER.

Note: Model 851-D units whose serial numbers are less than 6998 must be returned to the factory for internal modification. Field modification is not recommended.

Once the top cover has been replaced by the Display Control, connect three BNC cables and digital interface cable as shown in Figure 2.1.

SECTION II

INSTALLATION

2.1 Introduction

This section contains information on unpacking, inspection, repackaging, storage, and installation of the 116 Display Control Accessory.

2.2 Unpacking and Inspection

Inspect accessory for shipping damage as soon as it is unpacked. Check for broken connectors; inspect cabinet and panel surfaces for dents and scratches. If the accessory is damaged in any way or fails to operate properly, notify the carrier immediately. For assistance of any kind, including help with instruments under warranty, contact your local Biomation representative or Biomation in Cupertino, California, U.S.A.

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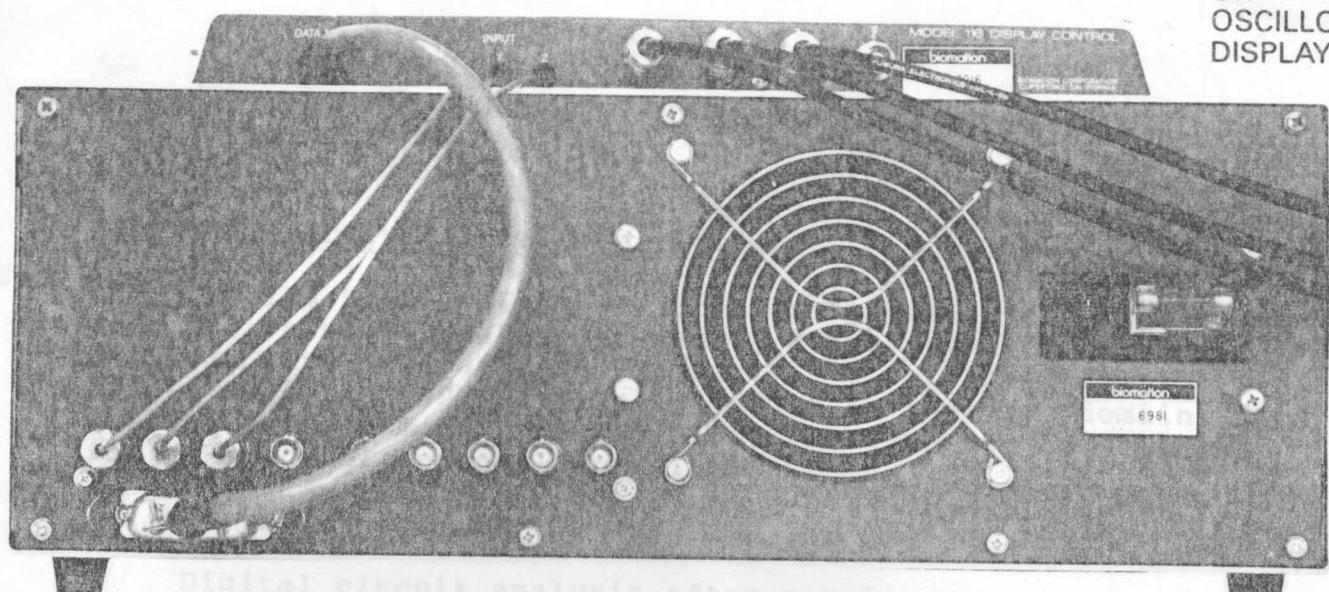
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Once the top cover has been replaced by the Display Control, connect three BNC cables and digital interface cable as shown in Figure 2.1.

TO CRT
OR
OSCILLOSCOPE
DISPLAY



Digital circuit analysis often requires precise and accurate transition time measurement on parallel signals including detection, with cause and effect relationships, of random narrow glitches. The familiar timing diagram is the most efficient and easily understood display format for this type of analysis. The movable display cursor and precise horizontal expansion of the Biomation Model 1650-D further enhances the timing diagram analysis. See Figure 3.1.

TO CRT OR
OSCILLOSCOPE
DISPLAY

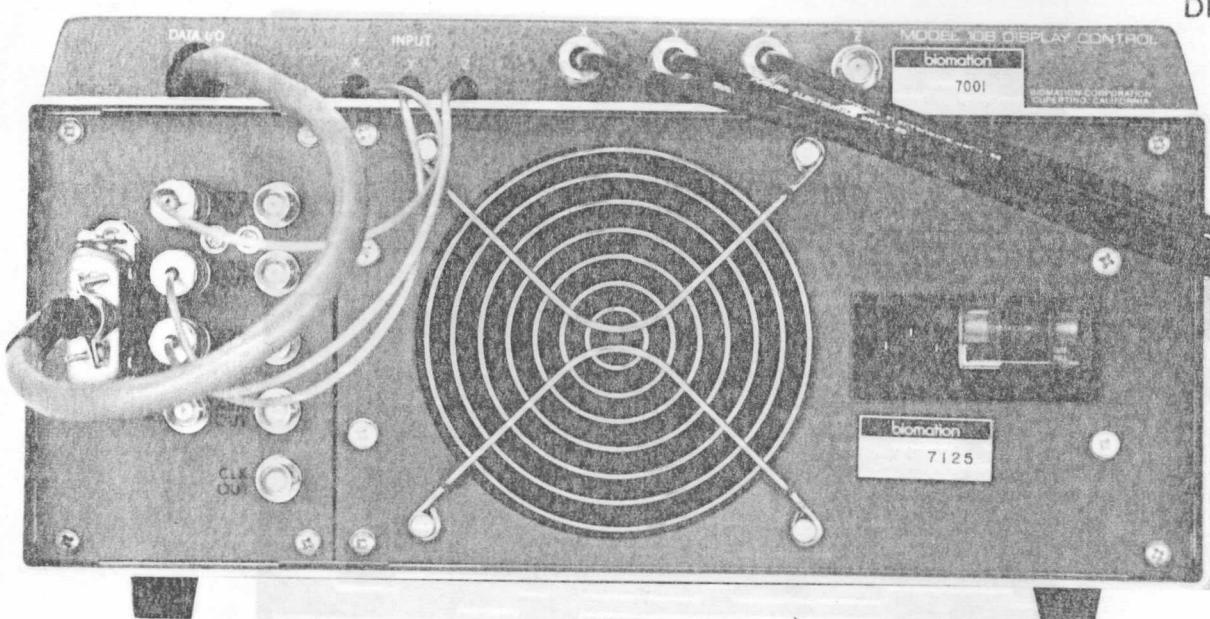


Figure 3.1

Time Domain Output Provides a Timing Diagram Presentation of the Model 1650-D.

Figure 2.1

The Interconnection Requirements for the (a) 116 Unit to the Model 1650-D and (b) for the 108 Unit to the Model 851-D.

3.1.2 Data Domain

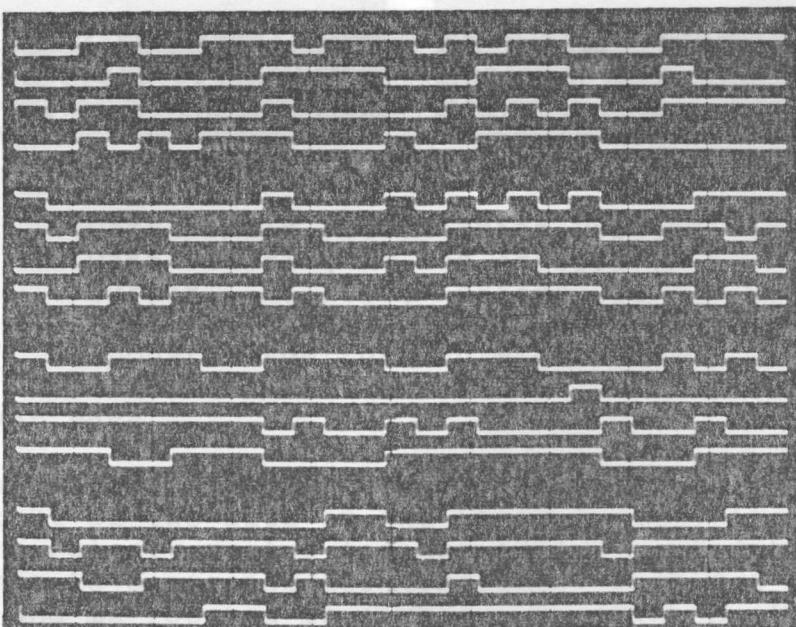
For analysis of logic SECTION III one-zero truth table display format is often desired. A hexadecimal or octal representation is a PRINCIPLES OF OPERATION analysis of this data. Selection of the data format on the 116 Display Control provides a list of 16 of the recorded data words. The word at the top of the display is the cursor word from the timing

3.1 Basic Functional Description

The 116 Display Control Accessory provides the Model 1650-D with the valuable feature of memory format control and digital analysis with a separate hold memory. The Display Control allows selection of the display format in the time domain, data domain, and map mode. In addition, the data may be selected for hexadecimal or octal translation.

3.1.1 Time Domain

Digital circuit analysis often requires precise and accurate transition time measurement on parallel signals including detection, with cause and effect relationships, of random narrow glitches. The familiar timing diagram is the most efficient and easily understood display format for this type of analysis. The movable display cursor and precise horizontal expansion of the Biomation Model 1650-D further enhances the timing diagram analysis. See Figure 3.1.



3.1.3 Data Domain

The memory format control allows the user to select the pattern output by the 116 Display Control. This is performed by selecting the appropriate address lines. An address line is a dot on the memory word, and it represents the CPT. This allows rapid selection of specific addresses.

Figure 3.1. Time Domain Output Provides a Timing Diagram Presentation of the Model 1650-D.

unique picture of the logic circuit operation. Aberrant operation can often be quickly spotted because a subtle data change will often result in a dramatic alteration in the map. See Figure 3.3.

3.1.2 Data Domain

For analysis of program data, a one-zero truth table display format is often desirable. A hexadecimal or octal representation is also a big aid in the analysis of this data. Selection of the data format on the 116 Display Control produces a list of 16 of the recorded data words. The word at the top of the display is the cursor word from the timing diagram presentation. This gives the ability to "scroll" through the entire 508 recorded words with the cursor control and analyze any 16 data words at a time. Each data word is represented by the decimal location in the memory (000 to 508), the binary data (16) bits, and by the hexadecimal or octal representation of this data. See Figure 3.2.

001	0010	0110	1001	0010	2692
002	0000	1000	1001	0011	0893
003	0000	1000	1001	0100	0894
004	1000	0110	1011	0100	86B1
005	0000	1000	1001	0100	0894
006	1000	1100	1001	0101	8C95
007	0101	0101	1010	0000	55A0
008	0010	0000	1010	0001	20A1
009	1000	1100	1001	0101	8C95
010	0000	0011	1001	0110	0396
011	1110	0000	1001	0111	E097
012	0010	0110	1011	0000	26B8
013	1011	0110	1011	0001	B6B1
014	0010	0000	1011	0010	20B2
015	1111	1111	1000	0000	FF80
016	1111	1111	1000	0000	FF80

136	1	111	111	110	000	101	177605
137	0	001	101	011	111	111	015377
138	0	001	011	010	000	110	013206
139	1	000	010	010	000	111	102207
140	1	000	010	010	000	111	102207
141	0	000	111	110	100	000	007640
142	1	000	101	010	100	001	105241
143	0	011	000	010	100	010	030242
144	1	000	000	110	100	011	100643
145	0	011	101	010	100	100	035244
146	0	010	010	110	100	101	022845
147	0	000	010	010	100	110	002246
148	1	000	000	010	100	111	100247
149	0	101	010	000	001	011	052013
150	1	000	000	010	100	111	100247
151	1	101	100	100	001	000	151110

Figure 3.2

Data Domain Presentation Presents 16 Words of Data Starting at the Address of the 1650-D Cursor. Relative Address, 16-Bit Binary Word, and HEX or Octal Translation of Each Word Appears From Left to Right on the CRT Display.

3.1.3 Map Mode

The map mode of the 116 Display Control provides a dot pattern output of the data in the Logic Analyzer's memory. This is particularly useful for the analysis of data on the address lines to semiconductor memories. Each dot represents an address and is located in a unique position on the CRT. This allows rapid detection of illegal or illogical addresses in the data. In addition, this graphic presentation provides unique pictures of the operation of particular types of circuits. Aberrant operation can often be quickly spotted because a subtle data change will often result in a dramatic alteration in the map. See Figure 3.3.

001 0010 0110 1001 0010 2692

3.1.4 Comp

The Model 1000 Logic Analyzer has the capability to retain 16 words of memory. The Logic Analyzer for our application has a large memory of 508 words. A memory sweep has been programmed to transfer data from portions of memory to the display. Data transfer can be selected, binned, or all data. If the logic address and data do not agree, the cursor mode (Delayed Address) is used. A #B (the new address) is used to save data.

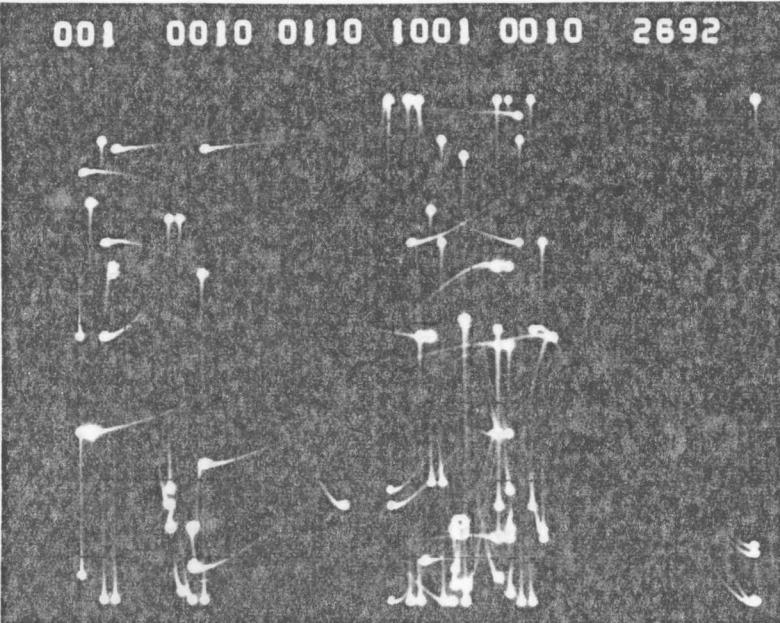


Figure 3.3

Map Mode Output Format Provides Readout of the 508 Word Analyzer Memory or the 16 Word Display Control Hold Memory. Note the Cursor Position is Circled; the Cursor Address and Data are Presented at the Top of the Display.

The map mode method of outputting the memory contents of the Logic Analyzer is constructed by using two digital-to-analog converters. Channels 1-8 are converted by one D/A converter that is then gated to drive the vertical axis of the display, while Channels 9-16 are converted by a second D/A to drive the X axis of the display as shown in Figure 3.4.

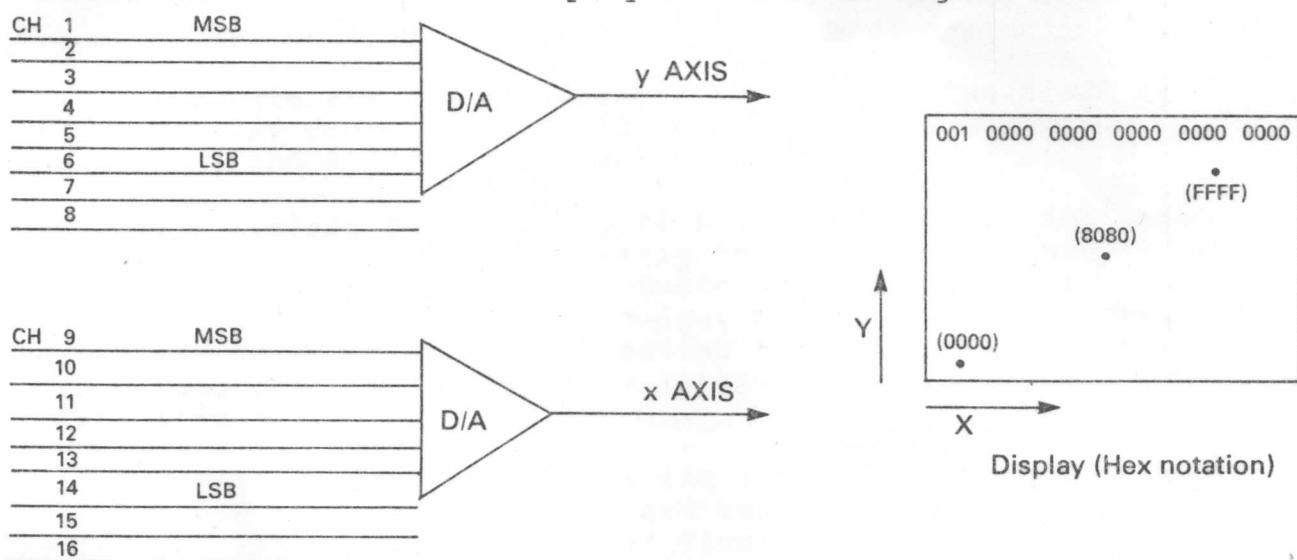


Figure 3.4

Construction of the Map Mode Display.

Note:

The two least significant bits of the display segments are not converted because the eye cannot perceive their effect. Simply moving the display cursor to a particular location allows full readout of their values.

3.1.4 Compare Functions

The Model 116 Display Control also provides the capability to retain 16 words of data from the memory of the Logic Analyzer for comparison to other portions of the analyzer's large memory or to subsequently recorded data. Once a record sweep has been completed, any 16 word portion may be transferred to the display control's B (hold) memory. Other portions or subsequent memory recordings may be compared to the data transferred to the B memory. When the compare function is selected, blinking occurs on the CRT for the data bits that do not agree. The compare function can further be used in an auto mode (Delayed Auto Record mode) to halt the record process when $A \neq B$ (the new recording no longer agrees with the previously saved data). Understanding of this section is essential to the successful use of this accessory.

4.2 Front Panel Controls

4.2.1 Arrangement of Controls

The controls of the Model 116 Display Control are arranged in three groups. Figure 4.1 shows the front panel. The three groups of controls are as follows:

- Storage A→B
- Display mode selection
- Memory and compare selection

4.2.2 Switch Types

Three unique types of switches are used on the front panel of the Display Control: interlocked pushbutton, momentary pushbutton, and alternate pushbutton.

The momentary pushbutton activates the function indicated when pressed, returning immediately in readiness for subsequent operation. The interlocked pushbutton switches provide alternate selection of display output modes, excluding other selections until chosen. By pressing the alternate action pushbutton, the "IN" position is latched. It is released by pressing it again.

The legends associated with the alternate action switch are observed as follows: there are two words beside each switch, separated by a horizontal line. The switch selects the upper function when in the "OUT" (unlatched) position and selects the lower function when in the "IN" (latched) position. In summation - upper function, button OUT; lower function, button IN.

SECTION IV

OPERATION

4.1 Introduction

This section identifies and describes front panel controls, rear panel connections, and typical operating procedures. Included are complete descriptions of the front panel controls, location and use, and the rear panel connector. A thorough understanding of this section is essential to the successful use of this accessory.

4.2 Front Panel Controls

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When the monitor reads sixteen words beginning at address location 00000000, it finds memory full of the following data:

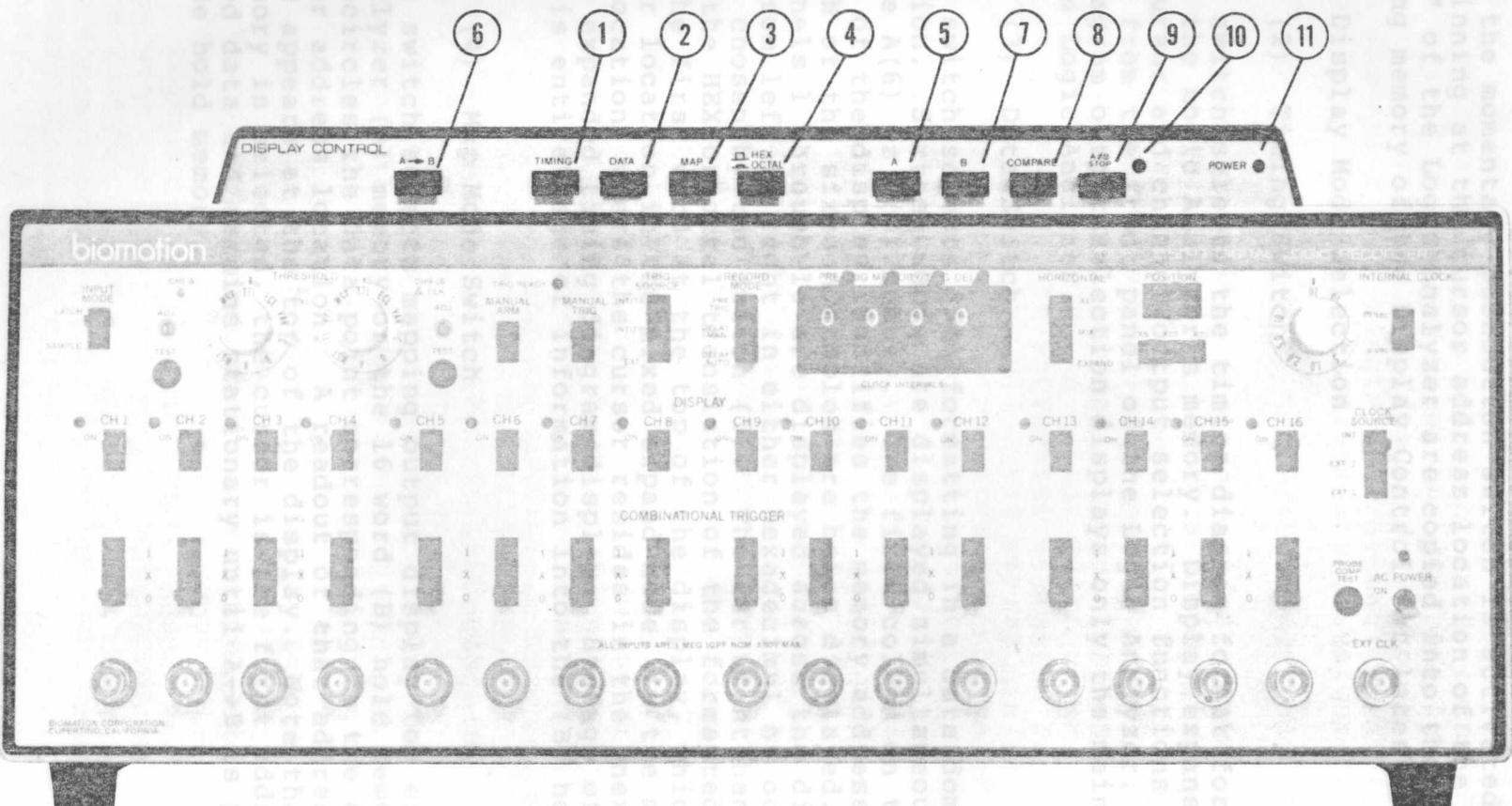


Figure 4.1 Front Panel of Model 116 Display Control

4.2.3 Storage A → B Switch

(1) A → B This switch selects translation and display formatting for a data domain presentation in either hexadecimal or octal. When the momentary pushbutton switch is activated, sixteen words beginning at the cursor address location of the main memory "A" of the Logic Analyzer are copied into the 16 word "B" holding memory of the Display Control for later analysis.

4.2.4 Display Mode Selection

(2) Timing Switch

This switch selects the timing diagram format for display output of the Logic Analyzer's memory. Display expansion as well as cursor and channel output selection functions are operative from the front panel of the Logic Analyzer. The timing diagram output selection displays only the main memory (A) of the Logic Analyzer.

(3) Data Switch

This switch selects data formatting in a data domain presentation. Sixteen words are displayed simultaneously from either the A(6) or B(7) memory. The first column on the left hand side of the display identifies the memory address from which each of the sixteen samples are being displayed. Data from Channels 1 through 16 are displayed across the display reading from left to right in either hexadecimal or octal and format as chosen by the switch (5). The far right hand column provides the HEX or octal translation of the formatted data words. The first word at the top of the display, which follows the cursor location in the mixed expand mode, is the memory address location, where the cursor resides in the unexpanded and fully expanded timing diagram display. Storage of A → B copies this entire page of information into the (B) hold of the memory.

(4) Map Mode Switch

This switch selects mapping output display for either the Logic Analyzer (A) memory or the 16 word (B) hold memory. The cursor encircles the data point corresponding to the data at the cursor address location. A readout of that address and the data word appears at the top of the display. Note that when the B memory is selected, the cursor is the first address of the stored data and remains stationary until A → B is pressed to update the hold memory.

This switch, engineered of this alternate action switch, used in conjunction with the Logic Analyzer's DELAY AUTO Record Mode, causes the analyzer to continuously update its memory, observing the selected trigger condition and comparing the 16 word B memory against the cursor selected 16 word portion of the A memory. If A = B, the auto arm function is executed,

(5) HEX/OCTAL Switch

This switch selects translation and display formatting for a data domain presentation in either hexadecimal or octal equivalents. With the switch in the OUT position, data is grouped in columns of 4 data bits each and translated with the left hand bit of each group being the most significant bit. The IN position arranges the data into five groups of 3 bits each with Channel 1 in a single bit column. Octal translation is provided in the far right column of each of these groups.

This 1 (6) A indicates that the Display Control accessory is receiving supply voltage from the Logic Analyzer.

The interlocked switch provides gating of the main memory of the Logic Analyzer for display as a timing diagram (2), data domain presentation (3), or map mode (4). In the timing diagram, precisely 500 bits of information are displayed with X1 expansion chosen. In the data domain, the entire memory may be explored by movement of the cursor switch. The scrolling speed is determined by the horizontal expansion factor chosen. A total of 508 words of the 512 total memory are accessible in this display mode. The last few words are not valid data and hence are not displayed. The memory map display also contains the 508 valid data points.

This 1 (7) B connect the display output of the Logic Analyzer to the Timing switch (3) on the front panel for output via (5).

This switch selects the 16 word hold memory for output. The stored information is available in both the data domain and map mode displays. Information stored in this hold memory is held independent of the Logic Analyzer's recording status.

This 1 (8) Compare Switch

This switch compares the A memory against the B hold memory. In the data domain (3) mode, comparison is made of the cursor address location and the subsequent 15 words against the 16 words of the hold memory. The differences blink in an easily read fashion for positive identification of the data variations. Comparison can easily be made between portions of a single program against subsequent record sweeps. Comparison in the map mode (4) allows comparison of the entire 508 words of the A memory against the 16 words of the B memory.

(9) (10) A ≠ B Stop

This function provides the unique capability of using the Logic Analyzer as a "watch dog" monitor for random failure analysis. Engagement of this alternate action switch, used in conjunction with the Logic Analyzer's DELAY AUTO Record Mode, causes the analyzer to continuously update its memory, observing the selected trigger condition and comparing the 16 word B memory against the cursor selected 16 word portion of the A memory. If A = B, the auto arm function is executed,

allowing the next trigger to be gated for a new record update. This cycling of arm, trigger, record, compare continues until ($A \neq B$) the A update no longer coincides with the stored B data. The light (10) is lit to indicate that the inequality has occurred. The auto arm function is disabled so that the last memory update may be analyzed by the user.

(11) Power Light

This light indicates that the Display Control accessory is receiving supply voltage from the Logic Analyzer.

4.3 Rear Panel Connectors

Figure 4.2 shows the rear panel connections.

(1) Data I/O Cable

This cable connects the Display Control accessory to the digital interface connector of the Logic Analyzer.

(2), (3), and (4) Input Cables

These cables connect the display output of the Logic Analyzer to the Timing switch (2) on the front panel for output via (5), (6), and (7) BNC connectors of the Control accessory.

(5) X OUT

A ramp waveform is output through this BNC connector for driving the horizontal axis of a CRT display or oscilloscope. This signal is synchronized with the Y OUT signal (6). The amplitude of the ramp is 1 V p-p with a 1 msec period for the Model 1650-D, and a 2 msec period for the Model 851-D.

(6) Y OUT

A repetitive 16 msec stair-step ramp drives the vertical axis of a CRT monitor or oscilloscope in the timing diagram mode. Data for each channel modulates each respective step level. Position and diddle scan technique is used to construct alphanumeric characters.

(7), (8) Z, \bar{Z} OUT

Z output is nominally a zero to +22 V pulse, 1 msec in duration for the Model 851-D and 0.5 msec in duration for the Model 1650-D, synchronized with the X output ramp for the CRT or oscilloscope blanking. \bar{Z} output has an inverted pulse of +5 V to zero.

4.4 Set Up Procedure

4.4.1 Initial Set Up

Connection Y, and Z or T output panel. Connect applicable amplitude horizontal display per division. Z pulse polarity circuitry of

Before voltage selector to ensure that the connector installed.

Connect as described in Service Manual in the timing section. Figure 6 shows

The digital information to address the single channel the effect of each channel. One does not have to see S. If the input hold will the other input

Note:

4.4.2 Control

Store to Logic Analyzer. Set cursor control display.

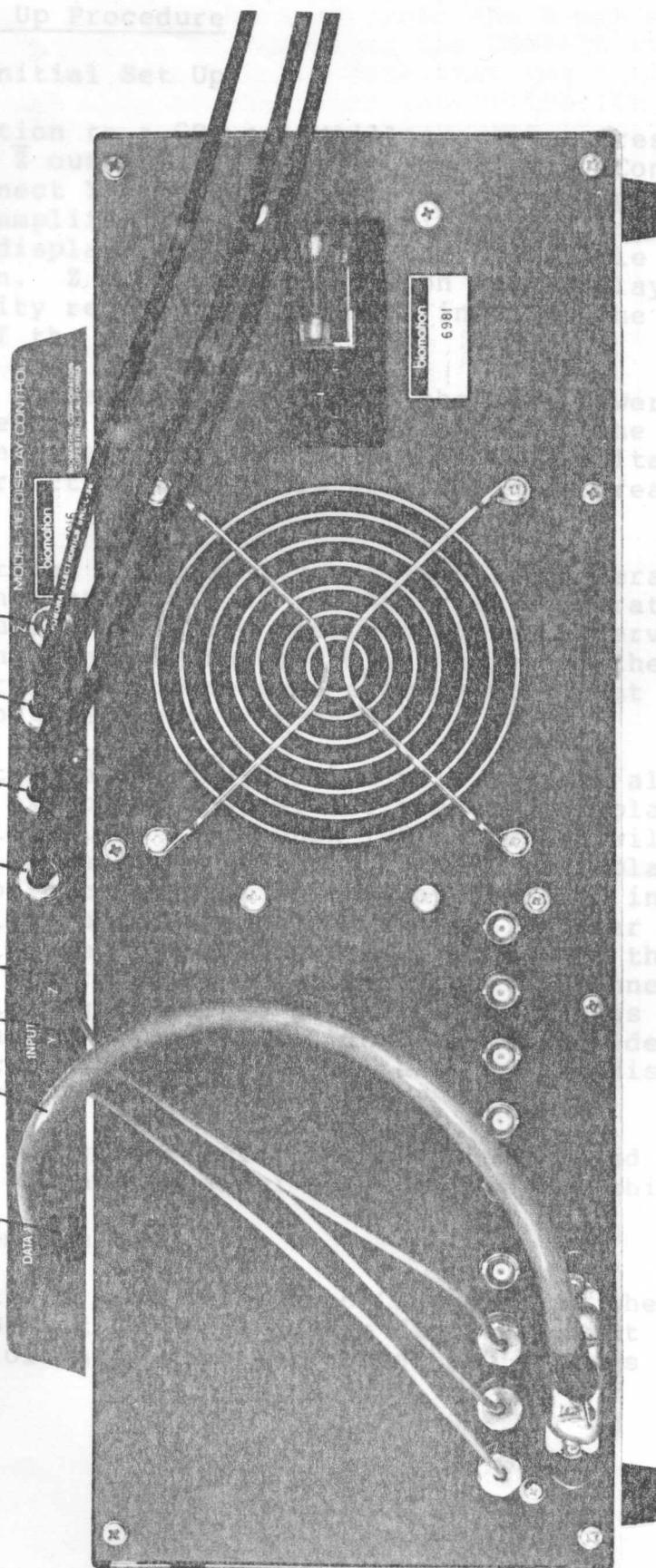


Figure 4.2 Rear Panel of 1650-D and 116 Display Control

4.4 Set Up Procedure

4.4.1 Initial Set Up

Connection to a CRT or oscilloscope requires use of the X, Y, and Z or \bar{Z} output signals from the Display Control rear panel. Connect Y into the vertical display input, setting the applicable amplifier to 0.1 V per division. Input X to the horizontal display, again setting the adjustable gain to 0.1 V per division. Z or \bar{Z} , depending upon the display blanking pulse polarity requirement, must be input to the blanking circuitry of the monitor used.

Before connecting the unit to the line power, check the voltage selector module on the rear panel of the Logic Analyzer to ensure that it is set to the proper line voltage. Be sure that the correct size fuse (as printed on the rear panel) is installed.

Connect the Logic Analyzer to a pulse generator as described in Section 4.4 of the Analyzer's Operating and Service Manual. Following that procedure, observe data output in the timing diagram, data, and map modes of the output. The timing diagram will correspond exactly with that shown in Figure 4.6 of the Analyzer's manual.

The data domain presentation will contain all zero information except on Channel 16, when the display is scrolled to address locations 51 through 100. The map will contain a single dot in the lower left corner of the display. To observe the effect of each channel in the map display, input a pulse to each channel sequentially. Two dots will appear on the map. One dot will move from the center left edge to the left corner to meet the other as the pulse is input to Channels 1 through 8. There will again be two points on the map as the pulse input is placed on Channel 9. The same effect described above will then occur on the horizontal axis of the display as the input is moved from Channels 9-16.

Note: Trigger selection must be changed to follow input channel selection during this exercise.

4.4.2 Compare Functions

Store the 5 μ sec pulse into Channel 1 of the Logic Analyzer. Select the data domain display format moving the cursor control until memory location 050 appears on the display.

Store that page (press A→B) into the B memory. Now move the cursor to location 100. Select the COMPARE mode and observe the differences blink. Note that the rate of alternate viewing provides ease of character identification. Switch to the map mode. In this COMPARE display, the 16 stored words are compared against 508 words from the main memory of the Logic Analyzer.

To observe operation of the A ≠ B STOP function, activate that switch, place the Logic Analyzer in the Delay Auto record mode, select zero delay, move the cursor to the 001 address, and record the 5 μ sec pulse. The red light above the A ≠ B Stop switch will light and subsequent pulsing of the input will be ignored until the A ≠ B is reset. Before resetting this control, however, store words 1-16 into the B memory (press A→B). Reset A ≠ B STOP and activate the repetitive 5 μ sec pulse. The light that indicates the location of an inequality will not light. Move the delay control by 10 sample increments until the record delay causes the data recorded to no longer compare (indicated by the red light). Examine the results.

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